Pattern Generator (Option 23)
MX364001B Software for Pattern Generator Data Write

(For MG3641A/3642A Synthesized Signal Generator)
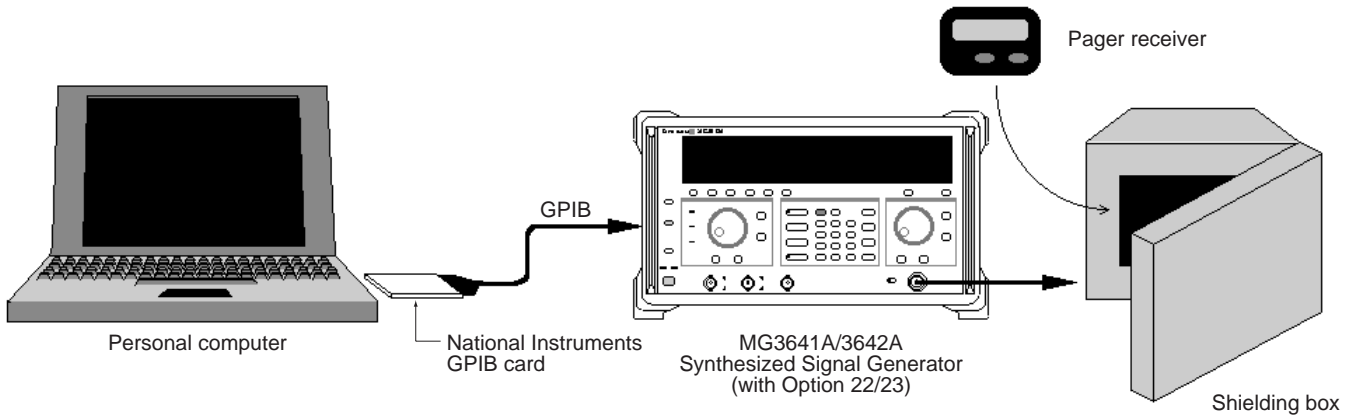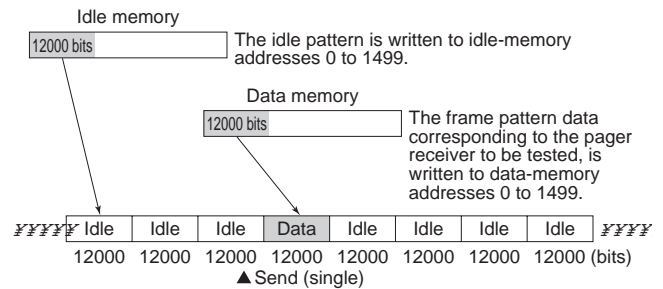
Pattern Generator (Option 23)

Installing the Pattern Generator (Option 23) in the MG3641A/3642A Synthesized Signal Generator enables the MG3641A/3642A to generate FSK-modulated or pulse-modulated signals from the internal modulation signal.∗
The Pattern Generator has four free-pattern memories where data can be written from a PC via the GPIB interface. It also has a fixed-pattern memory that generates the PN9/PN15 pseudorandom pattern and 0101 fixed pattern and outputs the data pattern synchronized to the internal clock generator frequency. When no data pattern is output, the idle pattern is output.

∗ The FSK Encoder (Option 22) is required for FSK modulation.
   The Pulse Modulator (Option 11) is required for pulse modulation.

● Data Output

When Single is selected, data output returns to the idle pattern after the data pattern is output once. When Continuous is selected, the data pattern is output continuously. In both cases, output of the idle pattern and data pattern is switched in synchrony with the respective pattern cycle.

Single

Idle	Idle	Idle	Data	Idle	Idle	Idle	Idle

▲Send

Continuous

Idle	Idle	Idle	Data	Data	Data	Data	Idle

▲Send   ▲Stop

● Output System

The Pattern Generator can output the data as 2-bit NRZ to support 4-level FSK modulation.

1-bit NRZ Output

Data is output sequentially to the Data 2^1 Output.

Idle	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
65535								
65534								
65533								
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
00003								
00002								
00001								
00000								

Data 2^1 ⟨ D0 ⟩ D1 ⟩ D2 ⟩ D3 ⟩ D4 ⟩ D5 ⟩ D6 ⟩

Clock

1/rate

Data 2^0 : 0 fixed

2-bit NRZ Output

Data is output sequentially to the Data 2^1 Output and Data 2^0 Output, two bits at a time. This system is for 4-level FSK modulation.

Address	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
65535								
65534								
65533								
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
00003								
00002								
00001								
00000								

Data 2^1 ⟨ D0 ⟩ D2 ⟩ D4 ⟩

Data 2^0 ⟨ D1 ⟩ D3 ⟩ D5 ⟩

Clock

2/rate

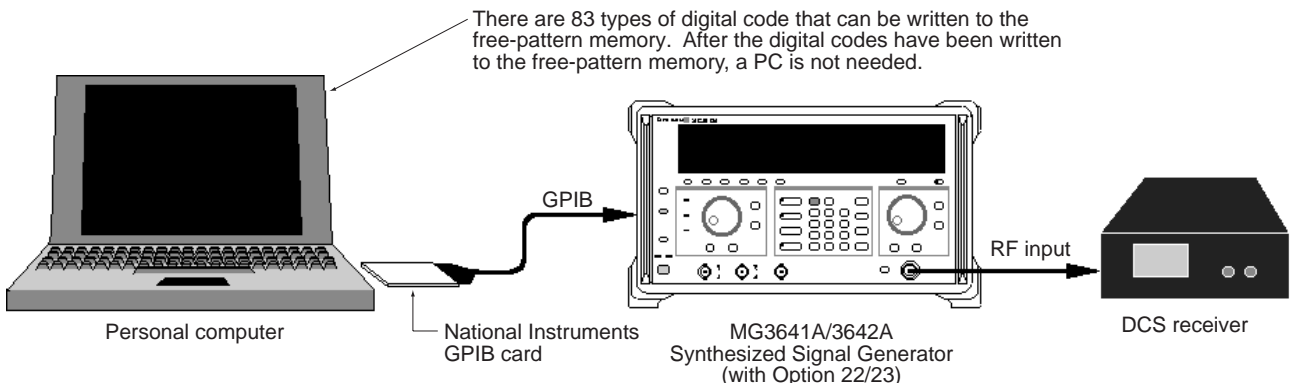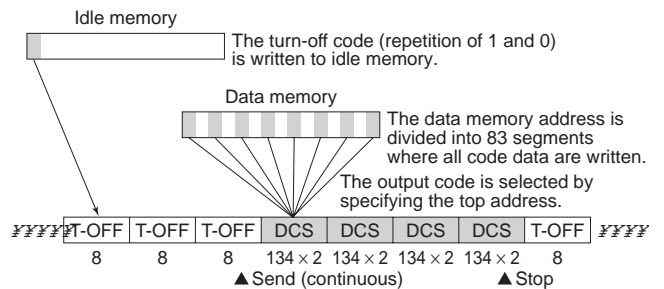# *Pattern Generator Application Example*

● **Pager Receiver Test**

The data pattern generated by the Pattern Generator (Option 23) is sent to the FSK Encoder (Option 22) where the it is modulated by 2-level or 4-level FSK modulation. The frame pattern data corresponding to the pager receiver to be tested is written to memory using a PC and the MX364001B software via the GPIB interface.
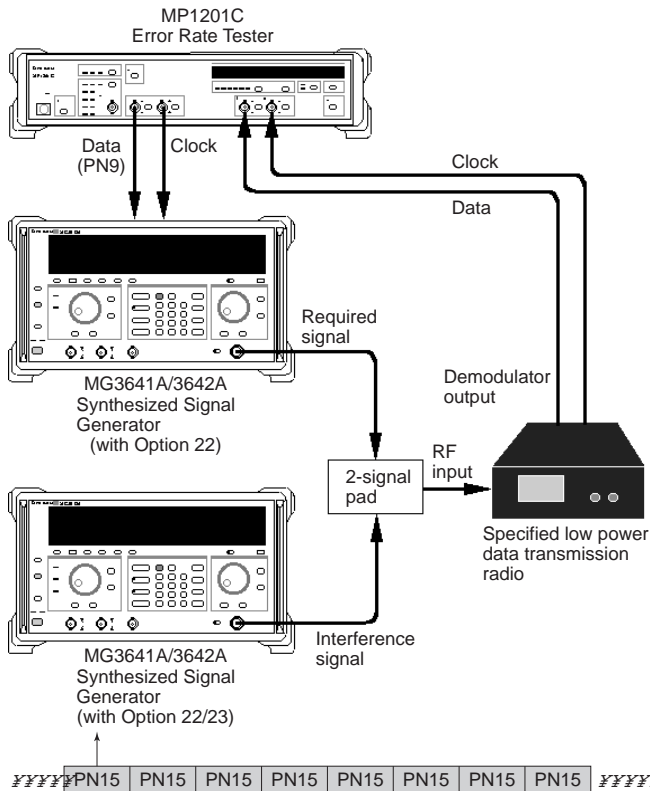
Idle memory

| 12000 bits | The idle pattern is written to idle-memory addresses 0 to 1499. |

Data memory

| 12000 bits | The frame pattern data corresponding to the pager receiver to be tested, is written to data-memory addresses 0 to 1499. |

¥¥¥¥¥ Idle	Idle	Idle	Data	Idle	Idle	Idle	Idle	¥¥¥¥
12000	12000	12000	12000	12000	12000	12000	12000 (bits)

▲ Send (single)

Pager receiver

Personal computer

National Instruments GPIB card

MG3641A/3642A Synthesized Signal Generator (with Option 22/23)

Shielding box

● **DCS (Digital Code Squelch) Radio Communications Test**

The data pattern generated by the Pattern Generator is sent to the FSK Encoder (Option 22) where it is modulated by 2-level FSK modulation. The data pattern to be written is generated by an external PC, and is written via the GPIB interface using the MX364001B software.

Idle memory

The turn-off code (repetition of 1 and 0) is written to idle memory.

Data memory

The data memory address is divided into 83 segments where all code data are written.

The output code is selected by specifying the top address.

¥¥¥¥¥T-OFF	T-OFF	T-OFF	DCS	DCS	DCS	DCS	T-OFF	¥¥¥¥
8	8	8	134×2	134×2	134×2	134×2	8

▲ Send (continuous)　　　　　　　▲ Stop

There are 83 types of digital code that can be written to the free-pattern memory. After the digital codes have been written to the free-pattern memory, a PC is not needed.

GPIB

RF input

Personal computer

National Instruments GPIB card

MG3641A/3642A Synthesized Signal Generator (with Option 22/23)

DCS receiver

● **Specified Low Power Data Transmission Radio Receiver Test**

The PN9-stage pseudorandom pattern generated as the required signal by the MP1201C Error Rate Tester is sent to the FSK Encoder (Option 22) where it is modulated by 2-level FSK modulation. Also the PN15-stage pseudorandom pattern generated as the interference signal by the Pattern Generator (Option 23) is sent to the FSK Encoder where it is modulated by 2-level FSK modulation. The error rate of the data modulated to the required signal is measured by the MP1201C Error Rate Tester.

MP1201C
Error Rate Tester

Data
(PN9)

Clock

Clock

Data

MG3641A/3642A
Synthesized Signal
Generator
(with Option 22)

Required
signal

Demodulator
output

2-signal
pad

RF
input

Specified low power
data transmission
radio

MG3641A/3642A
Synthesized Signal
Generator
(with Option 22/23)

Interference
signal

YYYY	PN15	PN15	PN15	PN15	PN15	PN15	PN15	PN15	YYYY

● **Generation of Pulse Modulation Signal**

The repetition pattern generated by the Pattern Generator (Option 23) is sent to the Pulse Modulator (Option 11) where it is pulse modulated. The required pattern is written to idle memory using either the fixed pattern of 01010101 (50% duty) or an external PC.

Coaxial cord

To Data 2[1] Output

To Pulse Input connector

MG3641A/3642A
Synthesized Signal Generator
(with Option 11/23)

Data
memory

0	1	0	1	0	1	1	1	0	1	0	0	1	1	0	1	0
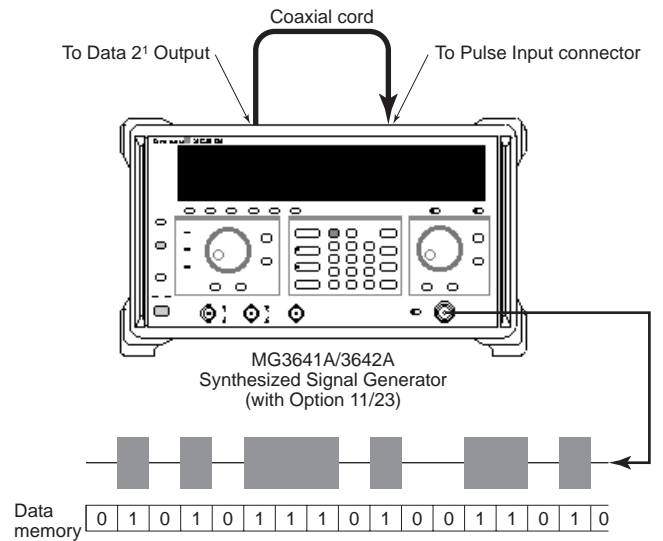
MX364001B Software for Pattern Generator Data Write

The MX364001B software enables writing of data easily from a PC to the Pattern Generator (Option 23) installed in the MG3641A/3642A Synthesized Signal Generator via the GPIB interface. The data written to the Pattern Generator (Option 23), is edited using a text editor on the PC. The edited data can be transferred to the MG3641A/3642A using this software.

● **Display Image**
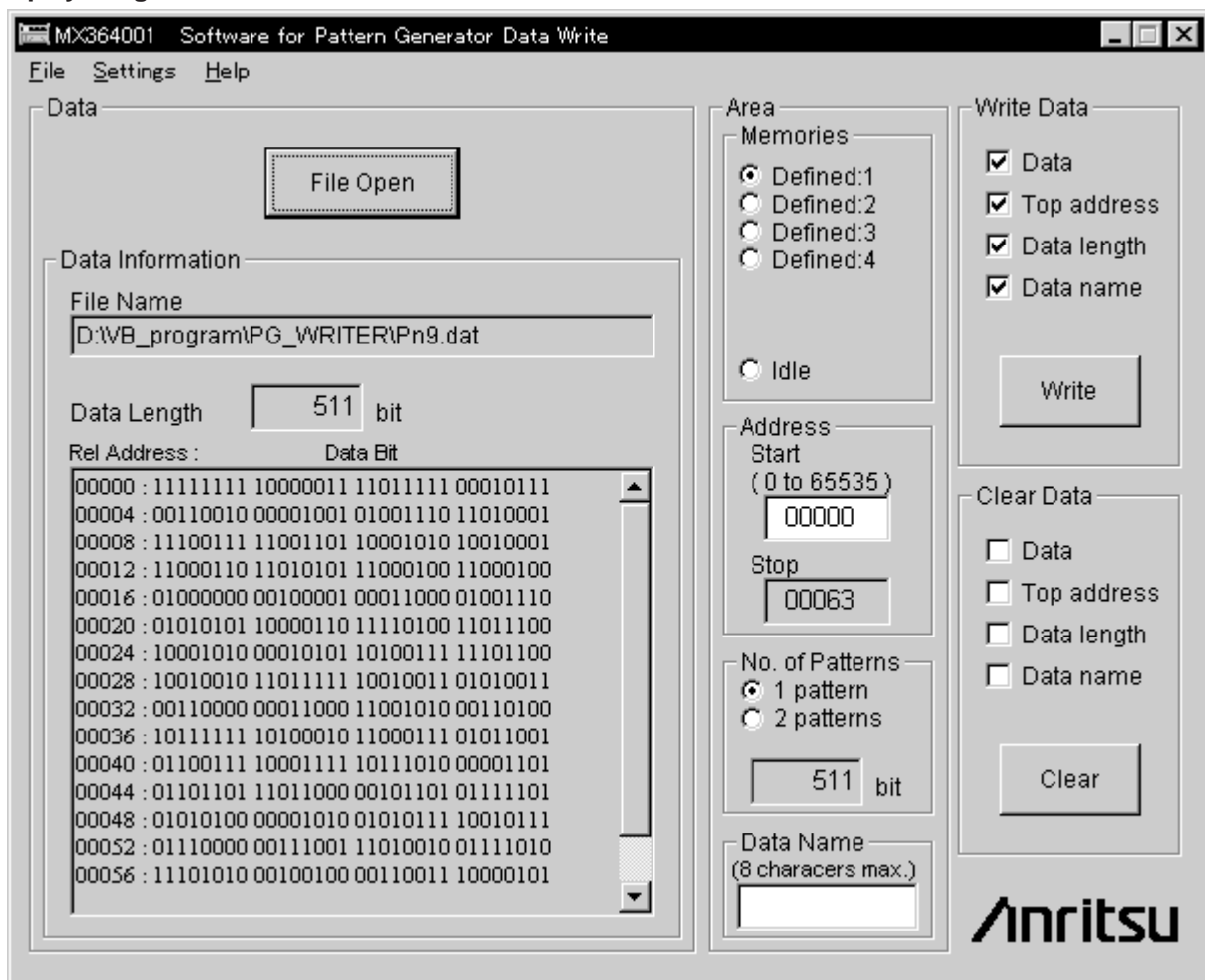
Step 1:
Reads data file

Step 2:
Specifies write area

Step 3:
Executes data write

Specifications

● **Pattern Generator (Option 23)**

Data pattern	Free	Number of memories: 4 (defined: 1 to 4)
		Memory capacity: 524,288 bits/memory
		Pattern output
		   Range: Top address and data bit length can be set for the respective free-pattern memories.
		   Top address setting range: 00000 to 65,535
		   Data bit length setting range: 2 to 524,288 bits (Final address of output: 65,535 or less)
		Memory: Saves 1-byte units via GPIB interface
		         Saves when pattern generator output off, or idle pattern being output

	Fixed	PN9 pseudorandom pattern (conforming to ITU-T V.52), PN15 pseudorandom pattern (conforming to ITU-T O.151), 01 fixed pattern

Idle pattern		Number of memories: 1 (idle)
		Memory capacity: 524,288 bits
		Pattern output
		   Range: The top address and data bit length can be set.
		   Top address setting range: 00000 to 65,535
		   Data bit length setting range: 2 to 524,288 bits (Final address of output: 65,535 or less.)
		Memory: Saves 1-byte units via GPIB interface
		         Saves when pattern generator output off

Output method		Single: Specified data pattern output once only (PN9 and PN15 are output twice.) Continuous: Specified data pattern output continuously When the data pattern is not output, the idle pattern is output continuously.
Output rate		Range: 1 to 99,999 bps (resolution: 1 bps) Accuracy: Same as reference oscillator of MG3641A/3642A

Output system		1-bit NRZ output (corresponding to binary data output):
		   Data is output to the Data 2^1 Output sequentially, one bit after another starting from the top bit.
		   The logic of Data 2^0 is fixed to 0.
		2-bit NRZ output (corresponding to quadrature data output):
		   Data is output to the Data 2^1 Output and Data 2^0 Output sequentially, two bits after another, starting from the top bit.

Output level		Data 2^0 Output: TTL level Data 2^1 Output: TTL level Clock Output: TTL level, rising

● **MX364001B Software for Pattern Generator Data Write**

Read-out data format	DOS text file
Write memory	Data pattern memory (defined: 1 to 4), idle pattern memory (idle)
Contents of write data	Pattern data: 2 to 524,288 bits/memory (text format file) Top address of output: 0 to 65,535 (any settable) Data bit length: 2 to 524,288 bits (Bit length of pattern data automatically calculated and written) Data name: Maximum eight characters (Idle pattern memory cannot be named.)
PC	IBM PC/AT compatible
Supporting OS	Microsoft® Windows 95
Interface	GPIB (National Instruments PCI-GPIB or PCMCIA-GPIB)

Ordering Information

Please specify the model/order number, name and quantity when ordering.

Model/Order No.	Name		Remarks
	Main frame		
MG3641A*1	Synthesized Signal Generator		125 kHz to 1040 MHz
MG3642A*1	Synthesized Signal Generator		125 kHz to 2080 MHz
	Optional units		
MG3641A/3642A-23	Pattern Generator		
	Application software		
MX364001B*2	Software for Pattern Generator Data Write		Microsoft® Windows 95
	Standard accessories		
W1389AE	MG3641A/3642A-23 operation manual:	1 pc	Supplied with MG3641/3642A-23
Z0351A	Label:	1 pc	Supplied with MG3641/3642A-23
W1459AE	MX364001B operation manual	1 pc	Supplied with MX364001B

*1 For the MG3641A/3642A in which the options are installed, and for the other options, refer to the individual catalog.

*2 The following items are required to use the MX364001B, and must be provided by the user.

IBM PC/AT Personal computer	486DX4 (75 MHz or higher), with memory of 32 MB or more (recommended) on which Windows 95 3.5-inch FD drive (for program installation)
GPIB interface	PCMCIA-GPIB or PCI-GPIB or equivalent GPIB interface manufactured by National Instruments Inc., supporting NI-488.2

Microsoft Windows 95 is a registered trademark of Microsoft Corporation in the USA and other countries.
IBM AT is a registered trademark of International Business Machines.
NI-488.2™ is a registered trademark of National Instruments Inc.

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